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# COMPUTER DIGEST

AND

USER'S BULLETIN

VOLUME I - ISSUE IV

OCTOBER 1975

EDITOR: N. WADSWORTH

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THIS IS THE LAST ISSUE OF THE "SCELBI COMPUTER DIGEST & USER'S BULLETIN." IN THE JULY ISSUE WE NOTIFIED OUR READERS THAT THE DIGEST WOULD BE DISCONTINUED IF USER'S DID NOT SHOW CONSIDERABLY MORE INTEREST IN PARTICIPATING. DURING THE PAST THREE MONTHS WE DID RECEIVE SEVERAL LETTERS URGING US TO CONTINUE PUBLICATION. TWO OF THESE LETTERS CONTAINED CONTRIBUTIONS. THOSE CONTRIBUTIONS ARE INCLUDED IN THIS ISSUE. SEVERAL MORE LETTERS INDICATED "INTENT," BUT AS OF THE PUBLICATION DATE THERE WAS NO FOLLOW UP. THESE FIGURES REPRESENT BUT A TINY PERCENT OF THE SUBSCRIBERS!

THE CONCLUSION WE REACH IS THE OBVIOUS ONE. PEOPLE ARE INTERESTED IN RECEIVING INFORMATION ON THE SUBJECT. FEW, HOWEVER, ARE IN A POSITION (FOR WHATEVER REASON) TO PROVIDE THE INFORMATION DESIRED BY OTHERS.

SCELBI IS WELL EQUIPPED TO PROVIDE INFORMATION AND PRODUCE PUBLICATIONS ON THE SUBJECT. WE CURRENTLY HAVE FIVE MANUALS AVAILABLE, WHICH WE HOPE OUR DIGEST READERS HAVE RECEIVED INFORMATION ON. WE ARE PLANNING MANY MORE SUCH PUBLICATIONS IN THE FUTURE. WE PLAN ON KEEPING OUR PREVIOUS "DIGEST" SUBSCRIBERS INFORMED AS THESE PUBLICATIONS BECOME AVAILABLE.

WE ARE, HOWEVER, DISCONTINUING THE PUBLICATION OF THE "DIGEST." PRODUCING A BULLETIN OF THE NATURE WE WANTED IT TO BE DID NOT WORK. WE HAD INTENDED IT TO BE ESSENTIALLY A "SERVICE" AND HAD PRICED IT HOPEFULLY TO BREAK EVEN (WE LOST). WE MADE EVERY ATTEMPT TO KEEP IT NON COMMERCIAL SO THAT USER'S WOULD BE FREE TO DISCUSS OTHER PRODUCTS, OR CRITICIZE OUR PRODUCTS. WE WANTED TO PROVIDE A VEHICLE FOR COMPUTER ENTHUSIAST TO EXCHANGE IDEAS THROUGH. WE ENDED UP PRODUCING ESSENTIALLY ANOTHER "PUBLICATION" WRITTEN MOSTLY BY OUR OWN STAFF AT COSTS FAR ABOVE WHAT THE PRODUCT WAS PRICED AT. WE CANNOT, REGRETFULLY, CONTINUE TO OPERATE ON THAT BASIS.

FORTUNATELY, FOR THOSE THAT DESIRE TO RECEIVE A WIDE RANGE OF RELATIVELY SHORT ARTICLES ON THE USE OF SMALL COMPUTER SYSTEMS, THERE IS A NEW, FULL FLEDGED MAGAZINE NOW AVAILABLE CALLED "BYTE." THIS MAGAZINE IS DEVOTED EXCLUSIVELY TO THE SMALL SYSTEMS ENTHUSIAST AND IS GEARED TO PRESENT THE TYPE OF ARTICLES WE TRIED TO PRESENT IN THE DIGEST. AFTER JUST THREE MONTHS OF OPERATION IT'S CIRCULATION IS REPORTED TO BE IN EXCESS OF 80,000! THE PUBLICATION COVERS A WIDE RANGE OF TOPICS WE FEEL MOST OF OUR FORMER DIGEST READERS WOULD BE INTERESTED IN. MANY LEADING AUTHORS IN THE FIELD ARE FEATURED IN THE MAGAZINE. (IN FACT, YOU WILL EVEN FIND ARTICLES BY MEMBERS OF THE SCELBI STAFF FROM TIME-TO-TIME.) THE COST ON A SUBSCRIPTION BASIS IS JUST \$12.00 PER YEAR, WHICH, QUITE FRANKLY WE CONSIDER AN EXTREMELY REASONABLE PRICE. (NOPE - WE DO NOT HAVE ANY SPECIAL INTEREST IN THE MAGAZINE OTHER THAN THE FACT THAT WE ADVERTISE IN IT. WE ARE PLUGGING IT BECAUSE WE FEEL IT IS A MUCH NEEDED PUBLICATION AND IN A MUCH BETTER POSITION TO PROVIDE THE KIND OF SERVICE OUR DIGEST READERS HAVE INDICATED THEY WANTED.) SUBSCRIPTIONS MAY BE OBTAINED BY WRITING:

BYTE - SUBSCRIPTION DEPT.  
PETERBOROUGH  
NEW HAMPSHIRE 03458

TO OUR SUBSCRIBERS, AND ESPECIALLY THOSE WHO CONTRIBUTED ARTICLES, WE EXTEND OUR THANKS FOR HELPING US "MAKE A GO AT IT." MAY YOUR SYSTEMS RUN SMOOTHLY.

## BEWARE OF CHEAP MEMORIES!

A COMMON DESIRE OF THE SMALL SYSTEMS USER IS TO OBTAIN AS MUCH MEMORY FOR THE USER'S SYSTEM AS THE USER CAN AFFORD - OR THE SYSTEM IS ABLE TO HOLD.

IN THE QUEST TO FILL THIS DESIRE MANY SYSTEM OWNERS OFTEN PROCEED TO ACQUIRE ADDITIONAL MEMORY BY LOOKING FOR SUPPLIERS OFFERING MEMORY ELEMENTS AT THE LOWEST POSSIBLE PROCUREMENT COST. UNFORTUNATELY, THE LOWEST INITIAL PROCUREMENT COST MAY NOT RESULT IN THE USER SPENDING THE LEAST AMOUNT OF MONEY (TO SAY NOTHING OF TIME - WHICH TO MANY PEOPLE IS MONEY) IN THE LONG RUN.

SOME TESTS MADE AT SCELBI COMPUTER CONSULTING, INC., TEND TO INDICATE THAT MEMORY ELEMENTS WHICH CAN BE OBTAINED AT "TOO GOOD TO BE TRUE PRICES" ARE JUST THAT! UNFORTUNATELY, MANY OF THE PURCHASERS OF THESE MEMORY ELEMENTS ARE NOT IN A POSITION TO MAKE A GOOD DETERMINATION OF THE QUALITY OF THE DEVICES THEY ARE OBTAINING. AND INDEED, THE WIDE DIFFERENCES IN PRICES OF MEMORY DEVICES CURRENTLY AVAILABLE FROM VARIOUS SUPPLIERS CAN BE ACCOUNTED FOR BY THAT ELUSIVE TERM "QUALITY."

THE PURPOSE OF THIS ARTICLE IS TO DISCUSS SOME OF THE PARAMETERS THAT AFFECT "QUALITY" OF MEMORY DEVICES SO THAT THE NOVICE MIGHT GET A BETTER IDEA OF WHAT TO LOOK FOR, AND "BEWARE OF" WHEN PURCHASING MEMORY DEVICES. THE TERM "MEMORY DEVICES" IN THIS ARTICLE REFERS TO "RAM" (READ AND WRITE) SEMICONDUCTOR DEVICES SUCH AS THE COMMONLY AVAILABLE STATIC 1101 AND 2102 TYPES.

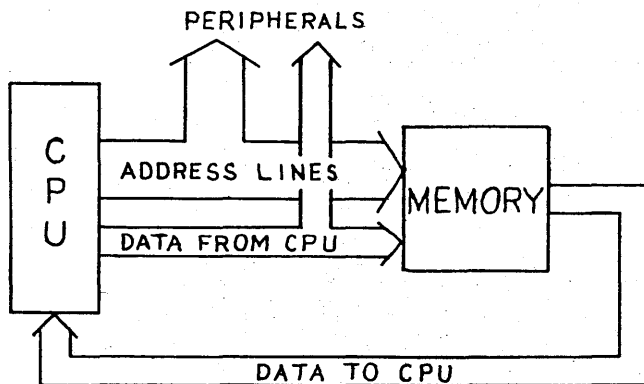
IT MIGHT HELP, AT THE START OF THIS ARTICLE TO POINT OUT, IN CLEAR TERMS, THE FACT THAT VIRTUALLY ALL THE DIFFERENCES IN PRICES ASSOCIATED WITH THESE MEMORY DEVICES CAN BE ATTRIBUTED TO "QUALITY." THERE IS TODAY, ONE CAN SEE BY READING THE VARIOUS "TRADE JOURNALS" A WIDE RANGE OF PRICES ASSOCIATED WITH THE DEVICES. FOR INSTANCE, TODAY ONE CAN SEE THE TYPE "2102" - A 1,024 BIT STATIC RAM DEVICE, BEING ADVERTISED IN SINGLE QUANTITY FROM A LOW OF \$2.00 TO AS MUCH AS \$10.00! THIS IS QUITE A PRICE SPREAD FOR AN ITEM THAT IS PRODUCED IN QUANTITIES OF HUNDREDS OF THOUSANDS! IT ALSO CAN MAKE QUITE A DIFFERENCE IF ONE IS BUYING, SAY A HUNDRED OR SO DEVICES TO ADD 12K OF MEMORY TO A SMALL COMPUTER SYSTEM! WHAT IS GOING ON? IS THERE SOME MYSTICAL SUPPLIER THAT HAS A CELLAR OF GOBLINS TURNING OUT MEMORY ELEMENTS AT FANTASTICALLY LOW COST WHO THEN SELL THESE "SPECIAL" DEVICES TO "SELECTED DEALERS" SO THAT THEY CAN PASS THESE DEVICES ON TO THE WAITING MULTITUDES AT "FANTASTIC" SAVINGS? NO. NOT HARDLY. THERE ARE RELATIVELY FEW FIRMS PRODUCING THESE DEVICES. FOR ONE THING, IT COSTS HUNDREDS OF THOUSANDS - AND INTO THE MILLIONS OF DOLLARS JUST TO EQUIP A FACTORY CAPABLE OF PRODUCING THESE DEVICES. THE TECHNOLOGY IS SUCH THAT THOSE THAT CAN AFFORD THE EQUIPMENT AND HAVE THE "KNOW-HOW" TO RUN THE PROCESS END UP HAVING VERY CLOSE TO THE SAME OVERALL COSTS TO PRODUCE "GOOD" DEVICES. THERE IS NO "FIVE TO ONE" EDGE AT THE MANUFACTURING LEVEL TO PRODUCE THE SAME QUALITY DEVICE. IF THERE WERE, THOSE ATTEMPTING TO SELL THE \$10.00 DEVICES WOULD BE OUT OF BUSINESS!

THE PRICE SPREAD THAT EXIST THEN, CAN BE PRETTY MUCH ATTRIBUTED TO QUALITY AND THE ABILITY (KNOWLEDGE) OF THE BUYERS TO DETERMINE WHAT THEY ARE PAYING FOR IN THIS REGARDS. THE BUYERS SHOULD THUS BE "EDUCATED" AS TO WHAT THEY ARE LIABLE TO BE RECEIVING (OR NOT RECEIVING) AS A FUNCTION OF THE PRICE THEY ARE PAYING.

FIRST OF ALL, IT MAY BE HELPFUL TO REALIZE HOW IMPORTANT MEMORY DEVICES ARE IN A COMPUTER SYSTEM. THEY ARE INDEED, VERY CRUCIAL ELEMENTS

IN A TYPICAL MINICOMPUTER SYSTEM. ALL THE INSTRUCTIONS IN A PROGRAM MUST BE HELD IN THE MEMORY ELEMENTS ALONG WITH ANY DATA THAT IS TO BE PROCESSED. IF MEMORY DOES NOT "REMEMBER" INSTRUCTIONS AND/OR DATA, THE COMPUTER CAN NOT OPERATE PROPERLY. A FAILURE OF ONE SINGLE BIT IN JUST ONE "WORD" IN MEMORY CAN BE JUST AS DEVASTATING TO THE OPERATION OF THE COMPUTER AS NOT HAVING ANY MEMORY AT ALL! THIS IS BECAUSE THE CHANGING OF ONE BIT IN AN INSTRUCTION CODE CAN RESULT IN THE COMPUTER PERFORMING AN ENTIRELY DIFFERENT OPERATION THAN THE ONE INTENDED - AND THIS CAN LEAD TO A "CHAIN REACTION" OF EVENTS WHICH CAN TOTALLY "DESTROY" THE OPERATION OF A PARTICULAR PROGRAM.

IN ADDITION TO THE FACT THAT A DEFECTIVE MEMORY ELEMENT CAN RESULT IN A PROGRAM OPERATING INCORRECTLY, IT IS ALSO IMPORTANT TO UNDERSTAND HOW A BAD MEMORY DEVICE MAY AFFECT OTHER PORTIONS OF THE COMPUTER SYSTEM. AS ILLUSTRATED IN THE DIAGRAM BELOW, IN A TYPICAL MINICOMPUTER SYSTEM THE MEMORY ELEMENTS OFTEN HAVE THEIR INPUTS (AND SOMETIMES THEIR OUTPUTS) TIED INTO A "BUSS" SYSTEM THAT GOES TO OTHER PORTIONS OF THE SYSTEM - SUCH AS I/O DEVICES. A DEFECTIVE INPUT TO A MEMORY ELEMENT IN SUCH A STRUCTURE CAN THUS EFFECT ANOTHER PORTION OF THE COMPUTER NOT DIRECTLY RELATED TO "MEMORY REFERENCE" OPERATIONS.



A WHILE AGO, SCELBI COMPUTER CONSULTING, INC., PURCHASED A FAIRLY LARGE AMOUNT OF RAM SEMICONDUCTOR DEVICES FROM VARIOUS SOURCES (ABOUT 1000 PIECES) AT THE CUT RATE PRICES ONE FREQUENTLY SEE'S ADVERTISED IN THE VARIOUS "POPULAR" TRADE JOURNALS. WE THEN PROCEEDED TO CONDUCT SOME TESTS TO SEE HOW GOOD THEY REALLY WERE AND TO ANALYZE THE VARIOUS FAILURE MODES FOUND, IF ANY.

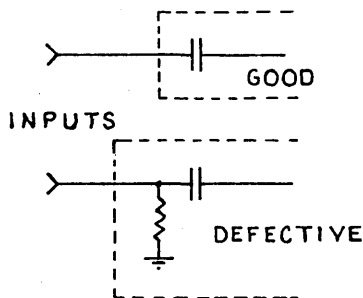
WE FOUND PLENTY OF DEFECTIVE DEVICES IN THESE LOTS. INITIAL INCOMING TEST, WHICH CONSISTED OF SIMPLY ATTEMPTING TO WRITE INTO AND TO THEN IMMEDIATELY READ DATA BACK OUT, RESULTED IN AN INITIAL FAILURE RATE THAT AVERAGED ABOUT FIFTEEN (15) PERCENT. (SOME LOTS HAD INITIAL FAILURE RATES AS HIGH AS 50 PERCENT - SOME LOTS AS LOW AS 8 PERCENT.) REMEMBER, THIS WAS THE FAILURE RATE ON JUST A SIMPLE GROSS TEST BEFORE TESTING FOR MORE SUBTLE DEFECTS OR OPERATION AFTER "BURN IN." MANY OF THE FAILURES NOTED DURING THIS TESTING STAGE WERE RELATED TO STUCK LOW INPUTS, INCORRECT ADDRESSING, DEVICES WITH EXCESSIVE CURRENT DRAIN THAT LITERALLY "BURNED UP" AND STUCK OUTPUTS. THEY WERE, TO PUT IT SIMPLY - GROSS FAILURES.

DEVICES THAT PASSED THE INITIAL INCOMING TEST, WERE THEN EXAMINED

FOR A SUBTLE DEFECT THAT CAN HAVE DEVASTATING EFFECTS IN A MINICOMPUTER SYSTEM BUT THAT ARE SELDOM SPOTTED BY NOVICES. THIS DEFECT HAS TO DO WITH THE INPUT "IMPEDANCE" (DYNAMIC RESISTANCE) OF THE MEMORY DEVICE.

SOME READERS MAY REALIZE THAT THE INPUT IMPEDANCE ON AN "MOS" (WHICH STANDS FOR "METAL OXIDE SILICON) DEVICE IS DESIGNED TO BE IN THE MEGOHM (MILLIONS OF OHMS) RANGE BECAUSE IT IS EFFECTIVELY A "CAPACITIVE" JUNCTION. WHAT IS SO IMPORTANT ABOUT THIS INPUT IMPEDANCE IF THE DEVICE IS ABLE TO APPEAR TO FUNCTION WHEN INSTALLED IN A SIMPLE TEST CIRCUIT? IN ORDER TO SEE THE IMPLICATIONS, ONE HAS TO CONSIDER HOW THE MEMORY ELEMENTS ARE TYPICALLY ARRANGED IN A MINICOMPUTER.

THE DIAGRAM BELOW REPRESENTS A SCHEMATIC OF THE INPUT TO A MOS MEMORY ELEMENT IN IT'S IDEALIZED FORM (A SIMPLE CAPACITOR OF SMALL VALUE - TYPICALLY 10 TO 15 PICOFARADS). BELOW THAT IS A SCHEMATIC OF AN INPUT THAT HAS A DEFECT RESULTING IN THE INPUT EXHIBITING A DC RESISTANCE THAT CAN BE AS LOW AS 10 K-OHMS OR LESS.



A MEMORY ELEMENT THAT HAS A "GOOD" (ESSENTIALLY CAPACITIVE) INPUT WILL REQUIRE VERY LITTLE DRIVING POWER FROM THE CIRCUIT THAT ACTIVATES THE INPUT - BE IT AN ADDRESS OR DATA LINE. WHEN THE INPUT LEVEL CHANGES, THE DRIVING CIRCUIT ONLY HAS TO "SOURCE" OR "SINK" ENOUGH CURRENT TO CHARGE OR DISCHARGE THE INPUT CAPACITANCE PLUS A VERY SMALL AMOUNT OF SO CALLED "LEAKAGE" CURRENT (IN THE ORDER OF NANO-AMPERES, OR MILLIONTHS OF AN AMPERE).

IF A DEVICE HAS A DEFECTIVE INPUT, HOWEVER, THE DRIVING CIRCUIT MUST THEN SUPPLY ADDITIONAL CURRENT REQUIRED BY THE EFFECTIVE RESISTANCE THAT IS REPRESENTED SCHEMATICALLY IN THE ABOVE DIAGRAM. THIS ADDITIONAL RESISTANCE CAN INCREASE THE DRIVER CURRENT DEMAND BY SEVERAL ORDERS OF MAGNITUDE!

A DRIVER MIGHT BE CAPABLE OF SUPPLYING ENOUGH CURRENT TO THE INPUT OF JUST ONE DEFECTIVE DEVICE. HOWEVER, LET'S LOOK AT HOW MEMORY DEVICES ARE TYPICALLY ARRANGED IN A COMPUTER SYSTEM.

THE ADDRESS AND DATA INPUT LINES TO MEMORY DEVICES ARE OFTEN TIED IN PARALLEL WITH MANY OTHER SUCH DEVICES. FOR INSTANCE, IN A SCLEBI-8H OR SCLEBI-8B MINICOMPUTER, THE LOW ADDRESS LINES AND THE DATA INPUT LINES MAY BE CONNECTED TO AS MANY AS 128 MEMORY DEVICES IN PARALLEL. THE CIRCUITS THAT DRIVE THESE INPUTS HAVE BEEN DESIGNED TO BE ABLE TO DRIVE ALL THOSE INPUTS PROVIDED THAT THEY ARE TRUE "MOS" INPUTS. SINCE TRUE "MOS" INPUTS ARE SUPPOSED TO BE ESSENTIALLY CAPACITIVE, THE DRIVING CIRCUIT NEED ONLY BE DESIGNED TO PROVIDE ENOUGH CURRENT TO SATISFY 128 RATHER SMALL CAPACITORS IN PARALLEL. FOR A FULL SYSTEM THIS CAPACITANCE IS EQUIVALENT TO 1 TO 2 NANOFARADS SINCE INDIVIDUAL CAPACITORS IN PARALLEL

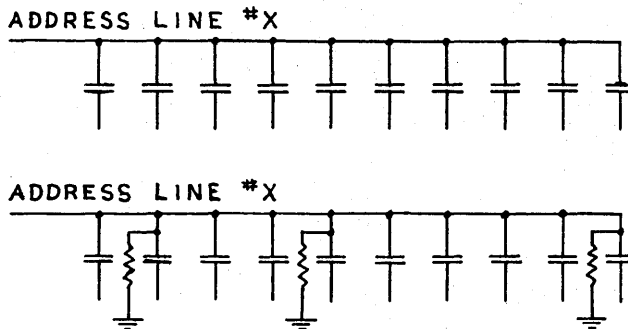
SIMPLY ADD IN VALUE.

THE FIGURE SHOWN NEXT ILLUSTRATES AN ADDRESS LINE IN A SYSTEM CONNECTED TO A NUMBER OF DEVICES IN PARALLEL. THE TOP ILLUSTRATION REPRESENTS A GROUP OF GOOD DEVICES. THE BOTTOM ILLUSTRATION DEPICTS A GROUP WITH SOME DEFECTIVE DEVICES.

NOTE WHAT HAPPENS IF THE INPUTS TO SEVERAL DEVICES ARE DEFECTIVE. THE TOTAL RESISTANCE ON THE LINE DECREASES RAPIDLY BECAUSE OF THE MANNER IN WHICH RESISTANCES IN PARALLEL BEHAVE. FOR INSTANCE, IF THE THREE DEFECTIVE INPUTS IN THE DIAGRAM EACH HAD A RESISTANCE OF 10 K-OHMS, THE TOTAL RESISTANCE ON THE ADDRESS LINE WOULD ONLY BE ABOUT 3.3 K-OHMS BECAUSE OF THE PARALLEL RESISTOR RELATIONSHIP:

$$R_P = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

AT SOME POINT, WITH DEFECTIVE INPUTS IN PARALLEL ON A LINE, THE CURRENT DEMAND WILL BECOME SO GREAT THAT THE DRIVER WILL BE "STARVED" AND UNABLE TO SUPPLY ENOUGH CURRENT TO PROVIDE THE REQUIRED VOLTAGE CHANGES TO THE INPUT OF THE DEVICES. THIS TYPE OF DEFECT, CAN, IN FACT, BE ESPECIALLY INSIDIOUS BECAUSE IT CAN CAUSE SYMPTOMS THAT CAN MAKE IT APPEAR AS THOUGH A PERFECTLY GOOD DEVICE IS MALFUNCTIONING. HOW? BECAUSE, THE VOLTAGE LEVEL SWINGS MAY BE LOWERED TO THE POINT WHERE SOME "GOOD" DEVICES CANNOT FUNCTION, BUT THE DEFECTIVE DEVICES (PARTLY BECAUSE OF THEIR DEFECTS) STILL DO FUNCTION. THIS CAN RESULT IN THE REMOVAL OF PERFECTLY GOOD DEVICES FROM A SYSTEM THROUGH MIS-DIAGNOSIS!



REMEMBER, SUCH DEFECTIVE DEVICES MAY WELL PASS AN OPERATIONAL TEST IN A TEST SET UP WHEN THEY ARE THE ONLY DEVICE BEING DRIVEN. WHAT IS AN EASY WAY FOR THE READER TO CHECK FOR THIS TYPE OF DEFECT? A VERY CRUDE TEST, BUT ONE THAT WORKS QUITE SATISFACTORILY CAN BE MADE WITH A SIMPLE OHM METER!

TO MAKE THE TEST, BE SURE AND USE AN OHM METER THAT USES A VERY LOW VOLTAGE BATTERY (1.5 TO 3 VOLTS). DO NOT USE AN OHM METER THAT USES HIGH VOLTAGE BATTERIES (SUCH AS 6, 9 OR 22 VOLTS - OR A "VTVM"). PLACE ONE LEAD ON A POWER SUPPLY PIN (SUCH AS PIN 5 ON A 1101 DEVICE) AND THE OTHER LEAD ON AN INPUT PIN. TAKE A READING AND THEN REVERSE THE LEADS. THE READING IN ONE DIRECTION MAY BE RELATIVELY LOW (REFLECTING AN INPUT PROTECTION DIODE) IN VALUE. THE OTHER READING SHOULD BE VERY HIGH - IN THE MEGOHM RANGE. IF IT IS NOT - BEWARE!

AN AVERAGE OF ABOUT FIVE PERCENT OF THE DEVICES EXAMINED IN THE TEST CONDUCTED ON THE DESCRIBED LOW COST ELEMENTS HAD ONE OR MORE DEFECTIVE INPUTS OF THE NATURE DESCRIBED. (SOME BATCHES HAD ONLY 1 OR 2 PERCENT, OTHERS RAN AS HIGH AS 40 PERCENT!)

ANOTHER COMMON PROBLEM THAT MAY BE ENCOUNTERED WITH LOW COST MEMORY ELEMENTS THAT IS NOT READILY DETECTED BY THE AVERAGE USER HAS TO DO WITH THE "SPEED" OF THE DEVICES. THIS "SPEED" PARAMETER HAS TO DO WITH THE AMOUNT OF TIME REQUIRED BY THE DEVICE AFTER AN "ADDRESS" HAS BEEN SET UP ON THE ADDRESS LINES BEFORE THE CELL ADDRESSED PROVIDES AN OUTPUT (OR IS READY TO HAVE IT'S CONTENTS CHANGED BY A "WRITE" OPERATION). THIS TIME IS USUALLY REFERRED TO AS THE "ACCESS" TIME OF THE DEVICE. IT IS GENERALLY SPECIFIED BY MANUFACTURERS TO BE IN THE RANGE OF FROM A FEW HUNDRED NANOSECONDS TO A MICROSECOND OR SO. THIS PARAMETER IS VERY MUCH A "QUALITY" RELATED ONE AND IS PARTLY DETERMINED BY THE PRECISENESS OF THE MANUFACTURING PROCESS. IN FACT, MANY MANUFACTURERS "GRADE" DEVICES WITHIN A FAMILY ACCORDING TO TESTS MADE AFTER A PRODUCTION RUN AND THEN SELL VARIOUS LOTS FROM THE SAME PRODUCTION RUN GRADED (AND PRICED!) ACCORDING TO HOW FAST THE ACCESS TIMES OF THE DEVICES ARE. FOR INSTANCE, IN THE "2102" FAMILY, ONE OFTEN SEES A MANUFACTURER SELL THE DEVICES BY ASSIGNING THEM "DASH NUMBERS" SUCH AS "2102-1," "2102-2," "2102-3" ETC., WHERE EACH DIFFERENT "DASH NUMBER" SIGNIFIES A PARTICULAR "MAXIMUM" OR WORST CASE "ACCESS" TIME FOR THE PARTS.

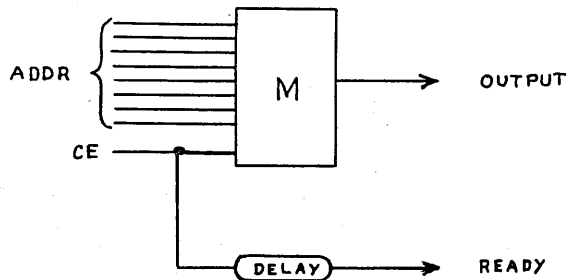
OF COURSE, LOW COST MEMORY ELEMENTS OFTEN DO NOT COME WITH "SPECIFICATION SHEETS" INDICATING THE WORST CASE ACCESS TIME AND THUS THE BUYER SHOULD BEWARE! THE SPEED OF SUCH DEVICES MAY BE MUCH WORSE THEN THE GENERALLY ACCEPTED MAXIMUM FOR SUCH DEVICES OF ABOUT 1 MICROSECOND! WITHOUT AN ELABORATE TEST SET UP, THERE IS VIRTUALLY NO WAY FOR THE BUYER TO DETERMINE THE SPEED OF THE DEVICES OTHER THAN BY "TRYING" THEM IN THE PURCHASERS SYSTEM. THEY MAY THEN SHOW UP AS SIMPLY A DEFECTIVE UNIT, OR THEY MAY CAUSE "TRANSIENT" OR "INTERMITTENT" PROBLEMS IF THE ACCESS TIME IS JUST AT THE MAXIMUM AT WHICH THE SYSTEM CAN TOLERATE. WHAT ACTUALLY HAPPENS WHEN SUCH A DEVICE IS IN A SYSTEM, IS THAT A SLOW DEVICE WILL NOT HAVE ENOUGH TIME TO "OUTPUT" THE VALUE AT A SELECTED ADDRESS BEFORE THE COMPUTER "READS" THE OUTPUT. THE COMPUTER MAY THEN RECEIVE AN INCORRECT VALUE FROM THAT MEMORY LOCATION.

WHILE ON THE SUBJECT OF SPEED IT MIGHT BE WORTH WHILE TO POINT OUT A SIDE ASPECT THAT SOME READERS DO NOT SEEM TO REALIZE. SOME POPULAR MINICOMPUTERS USE CPU'S THAT OPERATE FASTER THAN MANY MEMORY ELEMENTS ARE ABLE TO RESPOND TO. IN SUCH SYSTEMS, THE DESIGNERS INCLUDE CIRCUITS THAT DIRECT THE CPU TO "WAIT" UNTIL A MEMORY ELEMENT HAS HAD TIME TO ACCESS AN ADDRESS BEFORE ALLOWING THE CPU TO "SAMPLE" THE OUTPUT OF THE MEMORY. THIS IS ACCOMPLISHED THROUGH THE USE OF A "READY" LINE GOING TO THE CPU. UNFORTUNATELY, SOME USER'S SEEM TO HAVE THE IMPRESSION THAT THEY CAN USE ANY SPEED MEMORY BECAUSE THIS CIRCUITRY WILL AUTOMATICALLY WAIT UNTIL THE MEMORY ELEMENT IS READY. IN OTHER WORDS, THEY THINK THE MEMORY ELEMENTS THEMSELVES PROVIDE THE "READY" INDICATION. THIS IS NOT THE CASE. THE CIRCUIT THAT PROVIDES THE "READY" SIGNAL IS DESIGNED TO PROVIDE A FIXED DELAY FROM THE TIME A MEMORY ELEMENT IS INITIALLY ACCESSED SO THAT THE TYPE OF MEMORY PLANNED ON BEING USED IN THE SYSTEM WILL HAVE TIME TO PROVIDE AN OUTPUT BEFORE A "READY" SIGNAL IS FED BACK TO THE CPU. IT IS STILL POSSIBLE TO INSTALL MEMORY ELEMENTS THAT REQUIRE MORE TIME THAN THE DELAY CIRCUIT PROVIDES. TYPICALLY, SUCH "READY" CIRCUITS ARE DESIGNED TO PROVIDE ABOUT 1/2 A MICROSECOND DELAY SO THAT MEMORY DEVICES AS SLOW AS SAY, 1 MICROSECOND CAN BE USED IN A SYSTEM THAT MIGHT BE CAPABLE OF RUNNING AT FULL SPEED WITH MEMORIES THAT HAVE ACCESS TIMES OF 400 TO 500 NANOSECONDS. IF ONE PROCEEDS TO INSTALL MEMORY ELEMENTS WITH ACCESS TIMES OF, FOR INSTANCE, 2 MICROSECONDS, THEN THE "READY" DELAY CIRCUIT WILL NOT PROVIDE SUFFICIENT TIME AND THE SYS-

TEM WILL NOT OPERATE PROPERLY.

A PICTORIAL BELOW ILLUSTRATES HOW THE READY CIRCUITRY IS COMPLETELY INDEPENDENT OF THE MEMORY DEVICE. IN A TYPICAL SYSTEM, A SIGNAL IS FED TO A "DELAY" CIRCUIT WHENEVER A PARTICULAR MEMORY ELEMENT IS "ENABLED" BY THE "CHIP ENABLE" (CE) SIGNAL WHICH IS SENT AT THE SAME TIME AN ADDRESS APPEARS ON THE MEMORY ADDRESS LINES. THE DELAY CIRCUIT THEN PROVIDES A DELAY BEFORE ACTIVATING THE "READY" SIGNAL TO NOTIFY THE CPU THAT IT MAY "READ" THE DATA ON THE OUTPUT OF THE MEMORY DEVICE. (THE ACTUAL DELAY CIRCUITRY MAY RANGE FROM AN "RC" CONTROLLED GATE, TO A ONE-SHOT MULTIVIBRATOR, OR A CLOCKED FLIP-FLOP CIRCUIT DEPENDING ON THE ACTUAL DESIGN).

THE SCELBI-8H AND SCELBI-8B MINICOMPUTERS DO NOT UTILIZE A MEMORY READY SIGNAL AS NORMALLY SUPPLIED BECAUSE THE 8008 CPU PROVIDES PLENTY OF TIME FOR RELATIVELY SLOW MEMORY ELEMENTS (1 MICROSECOND ACCESS). HOWEVER, ONE SHOULD NOT ATTEMPT TO USE A MEMORY ELEMENT THAT REQUIRES MUCH MORE THAN THAT ACCESS TIME (AS MIGHT OCCUR WITH SECOND RATE MEMORY DEVICES) UNLESS ONE IS WILLING TO MODIFY THE SYSTEM TO INSTALL A SUITABLE MEMORY "READY" CIRCUIT.



DEVICES THAT PASSED THE INCOMING INITIAL TEST AND INPUT IMPEDANCE TESTS IN OUR SURVEY WERE THEN SUBJECTED TO A 72 HOUR "BURN IN" TEST CONSISTING OF CYCLING THE PARTS THROUGH WARM AND COLD TEMPERATURES (32 TO 200 DEGREES FAHRENHEIT AMBIENT) AND THEN OPERATING THEM UNDER SYSTEM CONDITIONS FOR THREE DAYS. THEY WERE THEN RETESTED. ANOTHER TWO PERCENT ON AN AVERAGE WERE FOUND DEFECTIVE AT THIS POINT.

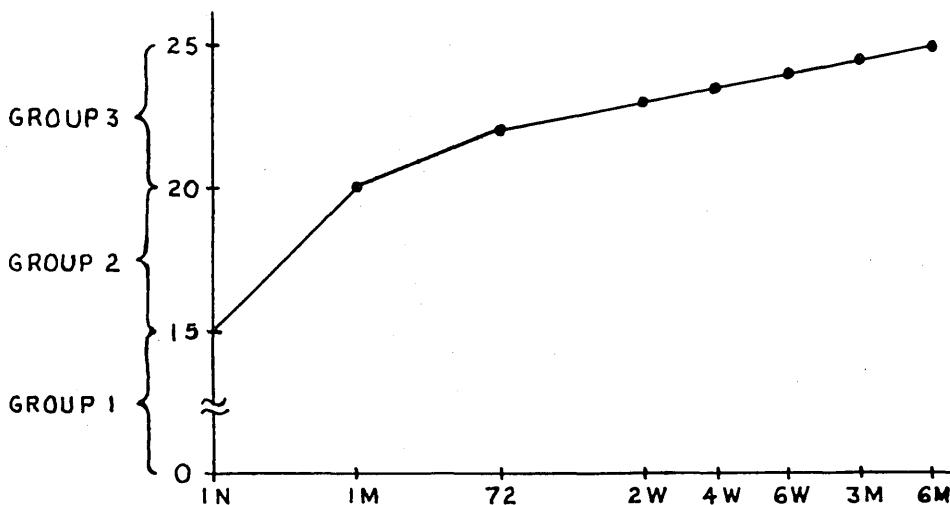
A COMMON FAILURE PATTERN WE NOTED AFTER "BURN IN" WAS THE INABILITY OF A MEMORY CELL TO "HOLD" A MEMORY STATE FOR A LONG PERIOD OF TIME. (LONG IN THIS CONTEXT BEING ABOUT FIVE SECONDS) HOWEVER, THE SAME CELL COULD RETAIN A VALUE FOR SEVERAL SECONDS. THIS PROBLEM WAS APPARENTLY CAUSED BY SOME SORT OF INTERNAL "LEAKAGE" CONDITION IN A CELL THAT WOULD EVENTUALLY CAUSE THE CELL TO CHANGE STATE, BUT WHICH DID NOT BECOME APPARANT IF THE CELL WAS REPEATEDLY "REFRESHED" BY READ AND WRITE OPERATIONS (EVEN THOUGH THE TYPE OF MEMORY ELEMENTS BEING TESTED WERE SPECIFIED AS BEING "STATIC" DEVICES NOT REQUIRING "REFRESHING" AS ANOTHER TYPE OF MEMORY DEVICES TERMED "DYNAMIC" MEMORIES DO). IN FACT, THE PROBLEM WAS SO PREVALENT THAT WE HAD TO MODIFY OUR TEST PROGRAM IN ORDER TO DETECT SUCH FAILURES BECAUSE OUR ORIGINAL TEST PROGRAMS CYCLED THROUGH MEMORY SO FAST THAT THEY EFFECTIVELY "REFRESHED" THESE DEFECTIVE CELLS BEFORE THEY HAD TIME TO SHOW THEIR WEAKNESS!

DEVICES THAT PASSED THE 72 HOUR BURN IN TEST WERE THEN INSTALLED IN A NUMBER OF SYSTEMS AND USED FOR MANY MONTHS. RECORDS WERE KEPT OF THE FAILURE RATES OF THESE DEVICES. IT WAS HORRIBLE. DURING THE NEXT SIX



MONTHS ANOTHER THREE PERCENT OF THE DEVICES FAILED. MOST DEVICE FAILURES WERE EITHER OF THE TYPE JUST DESCRIBED (WHERE A BIT WOULD CHANGE STATE) OR A COMPLETE FAILURE OF ONE OR MORE BITS IN A DEVICE TO RETAIN A PARTICULAR STATUS. THERE WERE SLIGHTLY MORE FAILURES DURING THE FIRST SIX TO EIGHT WEEKS OF OPERATION THAN IN LATER PERIODS. HOWEVER, A SIGNIFICANT NUMBER OF DEVICES CONTINUED TO FAIL AT RANDOM INTERVALS. SUCH A FAILURE RATE IS CERTAINLY FAR BEYOND WHAT ANY SERIOUS APPLICATIONS CAN TOLERATE. A COMPUTER SYSTEM WITH FROM 96 TO 128 MEMORY DEVICES (SUCH AS A 3 TO 4 K-WORD SCELBI-8H OR 12 TO 16 K-WORD SCELBI-8E) SHOULD BE ABLE TO OPERATE ON AN AVERAGE OF SEVERAL YEARS BEFORE ENCOUNTERING A MEMORY FAILURE IF GOOD QUALITY MEMORY ELEMENTS ARE INSTALLED. THE FAILURE RATES OBSERVED ON LOW COST MEMORY ELEMENTS CLEARLY INDICATE THEY ARE OF MUCH LOWER QUALITY.

A SUMMARY OF THE TEST RESULTS IS ILLUSTRATED IN THE GRAPH BELOW. THE GRAPH STARTS BY DEPICTING THE 15 PERCENT REJECT RATE FOUND AT INCOMING INSPECTION. THE POINT ON THE "X" AXIS MARKED "IM" SHOWS THE TOTAL PERCENTAGE AFTER TESTING THE INPUT IMPEDANCE. THE "X" AXIS THEN REFLECTS THE PERCENTAGE OF TOTAL FAILURES AFTER THE 72 HOUR BURN IN TEST. THE BALANCE OF THE GRAPH ILLUSTRATES HOW FAILURES CONTINUED AT A SIGNIFICANT RATE AS THE DEVICES WERE OPERATED UNDER NORMAL OPERATING CONDITIONS.



ALONG THE "Y" AXIS THE READER MAY NOTE THAT THE PERCENTAGE OF FAILURES WERE DIVIDED INTO THREE GROUPS. THE FIRST GROUP REPRESENTS THOSE DEVICES THAT WERE FOUND DEFECTIVE AT INCOMING INSPECTION AND WHICH ONE MIGHT BE ABLE TO GET THEIR MONEY BACK ON IF THEY PROMPTLY RETURNED THE UNITS TO THE VENDOR. (PROVIDING THE VENDOR OFFERED A MONEY BACK OR EXCHANGE POLICY - WHICH SOME PARTS VENDORS DO NOT!) THE SECOND GROUP REPRESENTS DEFECTIVE DEVICES THAT, FIRST OF ALL, THE UNINITIATED MIGHT NOT DISCOVER WERE DEFECTIVE UNTIL THEY WERE INSTALLED IN A SYSTEM - AND THEY THEY STILL MIGHT HAVE PROBLEMS LOCATING THE "GUILTY" UNITS AT THAT TIME. SECONDLY, IT IS A GROUP THAT ONE MIGHT HAVE A LITTLE MORE DIFFICULTY OBTAINING THEIR MONEY BACK ON - FOR SEVERAL REASONS. ONE BEING THAT SINCE THE DEVICE COULD PASS A SIMPLE TEST AND NO "SPEC SHEET" SPECIFYING AN INPUT IMPEDANCE WAS SUPPLIED WITH THE DEVICE - A VENDOR MIGHT FIGURE YOU

GOT WHAT YOU PAID FOR. A SECOND BEING THAT THIS TYPE OF PROBLEM MIGHT NOT BE DISCOVERED UNTIL THE WARRANTY PERIOD WAS OVER - OR THE DEVICE HAD BEEN INSTALLED (SOLDERED) IN A SYSTEM, IN WHICH CASE MOST VENDORS WOULD HAVE NO PART IN ACCEPTING THE RETURN FOR A REFUND.

THE THIRD GROUP REPRESENTS THE PERCENTAGE THAT ONE WOULD ALMOST CERTAINLY HAVE TO ACCEPT AS MONEY DOWN THE DRAIN - EITHER BECAUSE THE WARRANTY PERIOD HAD EXPIRED, OR THE DEVICE HAD BEEN INSTALLED IN A SYSTEM.

JUST HOW SERIOUS OF A PROBLEM CAN POOR QUALITY MEMORY ELEMENTS BE FOR THE INDIVIDUAL USER? IT DEPENDS, SOMEWHAT ON THE SYSTEM'S APPLICATION. IF THE USER IS PURELY A HOBBYIST, HAS PLENTY OF FREE TIME, IS WILLING AND ABLE TO CONDUCT THE TESTS, SEND IN DEFECTIVE PARTS AND WAIT FOR NEW ONES TO ARRIVE, AND LIVE WITH A DEVICE GOING BAD EVERY MONTH OR SO IN THE SYSTEM - WELL, PERHAPS IT IS SOME MONEY SAVED IN THE "HARD CASH" SENSE.

IF HOWEVER, THE USER IS AT ALL SERIOUS ABOUT THE SYSTEM'S USES, OR INTENDS ANY KIND OF BUSINESS APPLICATIONS, IT IS ALMOST CERTAINLY LIKELY TO BE A RISKY VENTURE. SETTING UP AND PERFORMING THE INITIAL TESTS AND BURN IN IS QUITE TIME CONSUMING. WAITING FOR REPLACEMENT PARTS TO ARRIVE CAN MEAN HAVING LESS THAN THE DESIRED SYSTEM. PERHAPS MORE DEVASTATING, HOWEVER, IS THE CONSTANT OCCURANCE OF A CHIP GOING BAD IN THE SYSTEM. HAVE YOU EVER SPENT 8 OR 10 HOURS TRYING TO "DEBUG" A PROGRAM UNDER DEVELOPMENT ONLY TO FINALLY ASCERTAIN THAT A BORDER LINE MEMORY ELEMENT WAS OCCASIONALLY DROPPING A BIT? HOW VALUABLE IS THAT TIME? OR, SUPPOSE A CHIP GOES BAD WHILE A MAILING LIST IS BEING SORTED AND A FEW HUNDRED CUSTOMER NAMES "DISAPPEAR" FROM YOUR SYSTEM BECAUSE THE COMPUTER RECEIVES AN INCORRECT INSTRUCTION AND PROCEEDS TO PERFORM A SYSTEM "WIPE OUT?" THE READER WILL NATURALLY HAVE TO BE THE JUDGE. THE POINT OF THIS ARTICLE HAS BEEN TO INFORM. TO PROVIDE SOME FIRST HAND EXPERIENCE IN THE FORM OF LESSONS WE HAVE LEARNED. (YOU DON'T THINK WE WENT OUT AND PURCHASED 1000 CHEAP RAM'S JUST SO WE COULD WRITE THIS ARTICLE DO YOU?)

WE HAVE FOUND IT PAYS IN THE LONG RUN TO BUY MEMORY ELEMENTS FROM TOP SUPPLIERS - EVEN THOUGH IT MEANS PAYING TOP PRICES. WHAT KIND OF FAILURE RATES DO WE EXPERIENCE WITH THOSE DEVICES? TO DATE - FROM ALL CAUSES - THE RATE HAS BEEN IN THE VICINITY OF 1/3 OF 1 PERCENT - OR TO PUT IT ANOTHER WAY, ABOUT 75 TIMES LESS THAN THE LOW COST UNITS WE TESTED. WHAT'S MORE, WE HAVE FOUND THAT VIRTUALLY ALL THE FAILURES HAVE BEEN DETECTED DURING INITIAL TESTING. FOR THIS "75 TIMES" IMPROVEMENT WE FIND WE ONLY HAVE TO PAY ABOUT TWICE THE "LOW COST" PRICE - AND THAT, READERS, IS A BARGAIN!

JUST HOW SERIOUS IS THE "CHEAP MEMORY" PROBLEM AMONG COMPUTER USERS? WELL, WE CAN TELL YOU THIS FACT: MORE THAN HALF OF ALL THE SCELBI-8H AND SCELBI-8B SYSTEMS RETURNED FOR SERVICE HAVE BEEN A DIRECT RESULT OF THE USER INSTALLING LOW COST MEMORIES! BY THE TIME THESE CUSTOMERS HAD PAID FOR ROUND TRIP SHIPMENT OF THEIR SYSTEM AND THE SERVICE CHARGE WE DOUBT IF VERY MANY OF THEM HAD SAVED ANY MONEY! TO SAY NOTHING OF THE INCONVENIENCE AND LOST TIME ON THEIR SYSTEMS.

THIS ARTICLE IS NOT A SUBTLE REQUEST FOR READER'S TO PURCHASE OUR MEMORY DEVICES - IT IS A SUGGESTION FOR READER'S TO SERIOUSLY CONSIDER PURCHASING "GOOD QUALITY" DEVICES FROM REPUTABLE MANUFACTURER'S REPRESENTATIVES.

IN ANY EVENT, AFTER READING THIS ARTICLE, YOU SHOULD KNOW ENOUGH TO  
B E W A R E !

AN OCTAL TERMINAL

BY

DAVID DAMERON  
402 E. O'KEEFE ST.  
E. PALO ALTO, CA. 94303

MR. DAMERON SENT IN THE SCHEMATIC FOR AN OCTAL TERMINAL HE DESIGNED WHICH IS ILLUSTRATED ON THE FOLLOWING PAGE. PIN NUMBERS ON THE I.C.S USED WERE NOT INCLUDED SO YOU WILL HAVE TO REFER TO A MANUFACTURER'S DEVICE HANDBOOK OR CONTACT MR. DAMERON. HE ALSO INCLUDED SOME PROGRAMS AND THE FOLLOWING COMMENTS.

"I HAVE FINISHED AN OCTAL TERMINAL WHICH OTHER USERS MIGHT BE INTERESTED IN. IN THE "READ" MODE, DIGITS 0 - 7 ARE ENTERED IN CYCLIC ORDER. WHEN A WORD IS TO BE ENTERED, THE "ENTER" KEY IS PRESSED WHICH LOCKS OUT THE DIGIT KEYS AND SETS "DATA READY" HIGH. TO ACKNOWLEDGE THE DATA WORD THE COMPUTER STROBES THE "DATA ACCEPT" WHICH RESETS THE COUNT FLIP-FLOP AND PLACES THE TERMINAL IN THE "WRITE" MODE. IN THE "WRITE" MODE, AN OUTPUT PORT IS DISPLAYED. TO SET THE TERMINAL IN THE "READ" MODE, ANY DIGIT KEY IS PRESSED."

THE FOLLOWING OPERATING PROGRAMS WERE INCLUDED BY MR. DAMERON.

```

/
003 000 103          TEST, INP 001          /INPUT PORT 1
003 001 044 004     NDI 004                /FLAG "DATA READY"
003 003 150 000 003 JTZ TEST                /TRY AGAIN FOR "DATA READY"
003 006 105         INP 002                /INPUT DATA
003 007 370         LMA                     /STORE IN MEMORY
003 010 141         OUT 020                 /ACCEPT DATA
003 011 060         INL                     /INCREASE POINTER
003 012 306         START, LAL              /PUT "L" INTO "A"
003 013 121         OUT 010                 /OUTPUT "L"
003 014 104 000 003 JMP TEST                /JUMP "TEST"
/

```

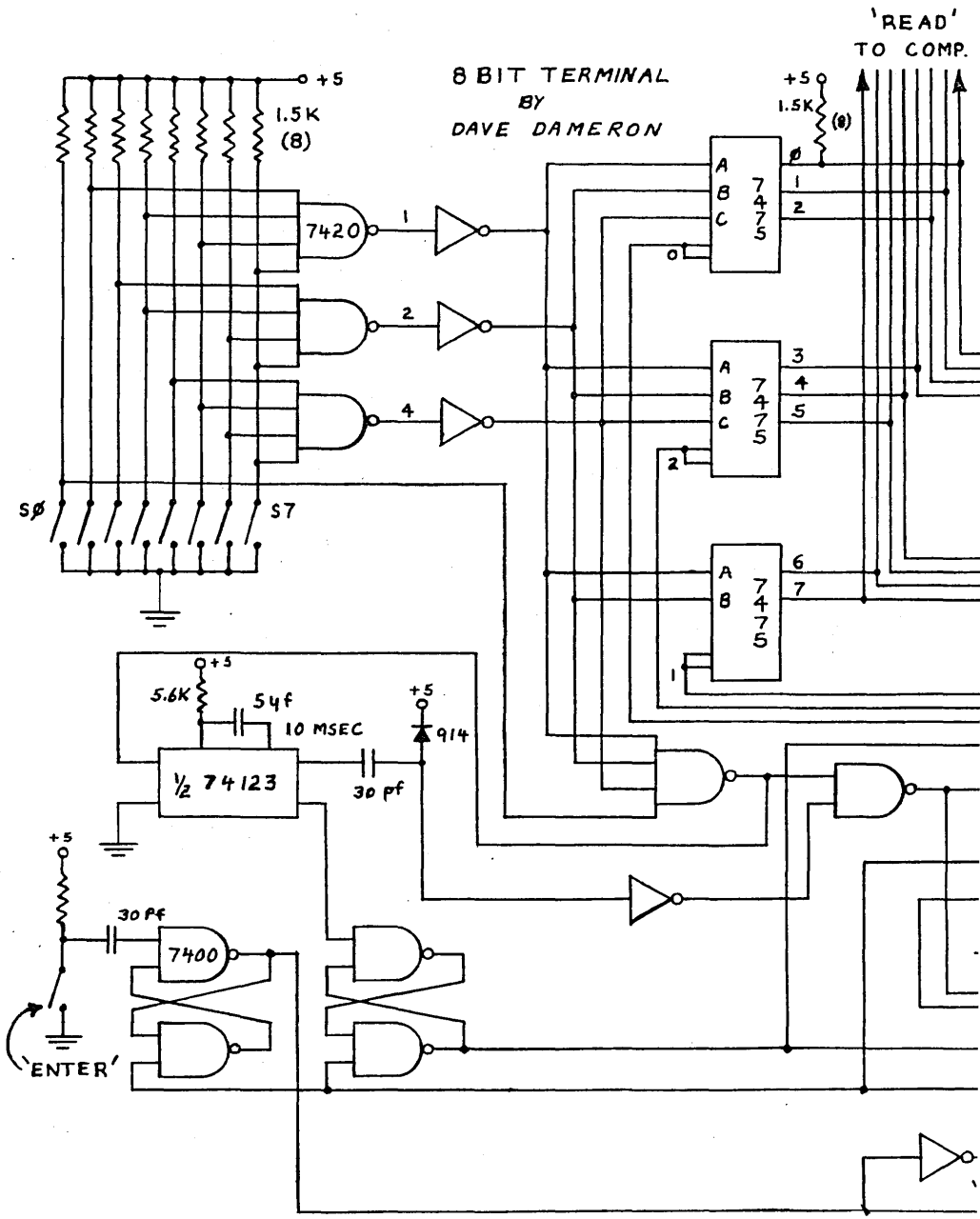
"TO USE THIS ROUTINE, JUMP TO "START" AT LOCATION 012 ON PAGE 03. THE LOCATION OF THE NEXT WORD IN MEMORY WILL BE VIEWED AT THE TERMINAL. ENTER THE DATA WORD, THEN PRESS "ENTER." THE WORD WILL BE STORED AND THE NEXT LOCATION WILL BE VIEWED. INTERRUPT TO TERMINATE THIS ROUTINE."

```

/
002 000 103          TEST, INP 001          /INPUT PORT 1
002 001 044 004     NDI 004                /FLAG "DATA READY" BIT B2
002 003 150 000 002 JTZ TEST                /TRY AGAIN FOR "DATA READY"
002 006 307         LAM                     /MOVE "M" TO "A"
002 007 141         OUT 020                 /CLEAR TERMINAL
002 010 121         OUT 010                 /OUTPUT WORD
002 011 060         INL                     /INCREMENT POINTER
002 012 104 000 002 JMP TEST                /JUMP "TEST"
/

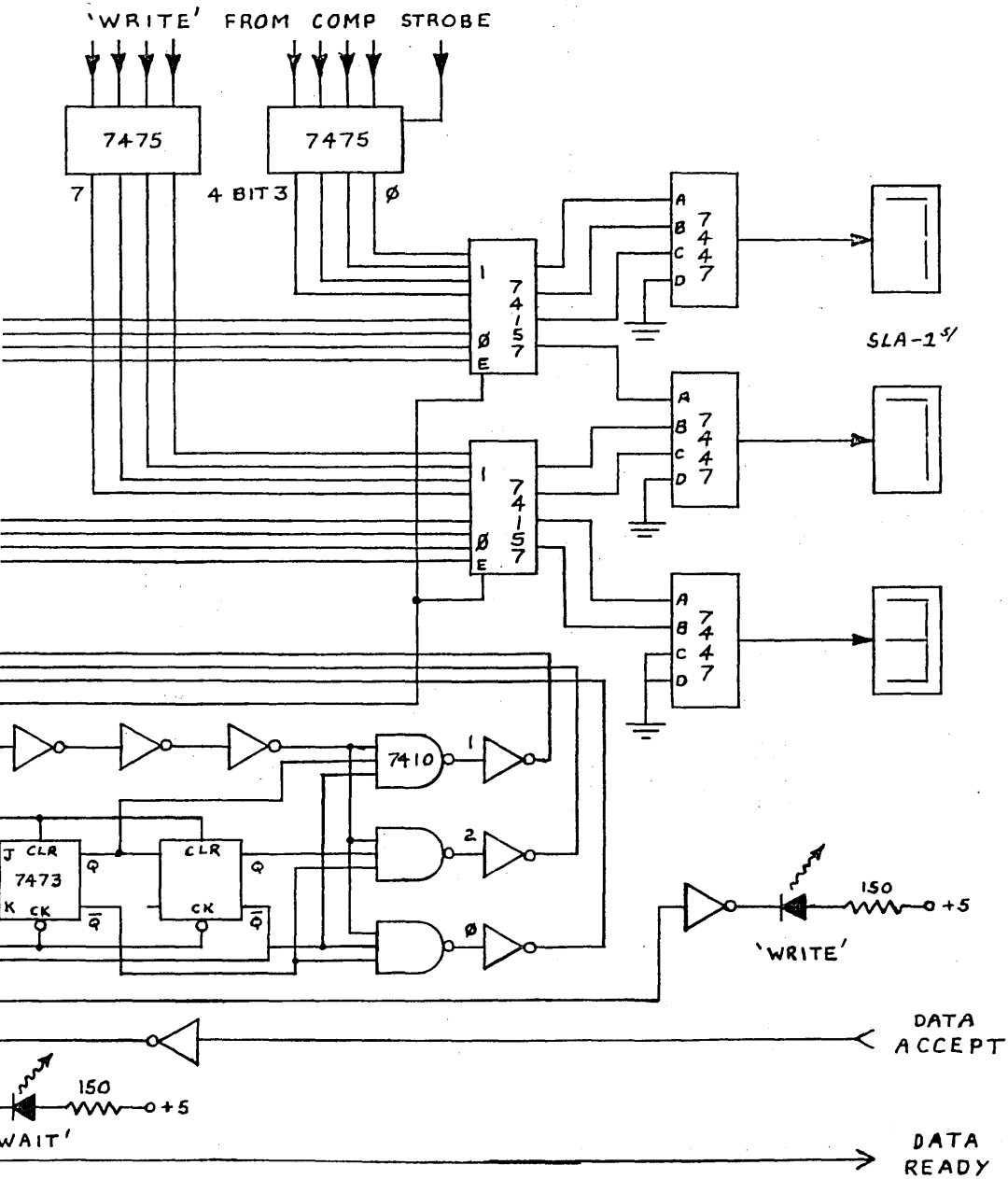
```

"PRESS "ENTER" TO DISPLAY SUCCESSIVE WORDS ON A PAGE. INTERRUPT TO TERMINATE THIS ROUTINE."



8 BIT TERMINAL  
BY  
DAVE DAMERON

'READ'  
TO COMP.



## A SIMPLE MAG TAPE FILE PROGRAM

IT IS OFTEN DESIRABLE TO USE A COMPUTER COUPLED TO A MASS STORAGE DEVICE SUCH AS A TAPE UNIT TO ACT AS A FILE SYSTEM. FOR INSTANCE, ONE MIGHT WANT TO MAINTAIN A LIST OF NAMES AND ADDRESSES FOR MAILING PURPOSES. PERIODICALLY, ONE MIGHT WANT TO PROCESS THE NAMES AND ADDRESSES AND SEND INFORMATION TO SELECTED INDIVIDUALS. A SIMPLE AUDIO CASSETTE MAG TAPE SYSTEM CAN BE USED FOR SUCH PURPOSES IF THE NUMBER OF "FILES" IS NOT TOO LARGE, AND THE DATA DOES NOT TO BE UPDATED ONCE IT HAS BEEN PLACED ON THE TAPE. (IF IT IS NECESSARY TO UPDATE FILES THEN A MORE SOPHISTICATED SYSTEM THAN THE ONE TO BE DESCRIBED HERE SHOULD BE USED, AND IT WOULD BE ADVISABLE TO USE MULTIPLE TAPE UNITS WITH FAST SEARCH CAPABILITY.) ONE CAN, HOWEVER, USING A SIMPLE AUDIO TAPE SYSTEM, DEVELOP A SYSTEM THAT WILL ALLOW CERTAIN "FILES" TO BE SELECTED, AND OTHER FILES TO BE SKIPPED WHEN THE DATA IS PROCESSED.

ALL THAT IS NEEDED TO DEVELOP A SIMPLE MAG TAPE FILE PROGRAM IS SOME SORT OF PROGRAM THAT WILL ALLOW DATA TO BE WRITTEN AS "BLOCKS" ON A TAPE AND ANOTHER PROGRAM THAT CAN READ IN THE BLOCKS. ONE CAN THEN SIMPLY SPECIFY A FORMAT FOR "BLOCKS" SO THAT A SUBROUTINE CAN SELECT CERTAIN KINDS OF INFORMATION FROM A "BLOCK" AND DETERMINE WHETHER THE INFORMATION IN THE BLOCK IS OF INTEREST OR WHETHER TO SKIP A BLOCK.

THE EXAMPLE TO BE PRESENTED HERE ILLUSTRATES THE SYSTEM FOR PROCESSING A LIST OF NAMES AND ADDRESSES BUT THE CONCEPT COULD BE APPLIED TO OTHER TYPES OF SIMILAR DATA HANDLING PROBLEMS.

THE FIRST STEP IN DEVELOPING SUCH A SYSTEM IS TO CREATE A PROGRAM THAT WILL ALLOW A BLOCK OR "FILE" OF DATA TO BE CREATED AND THEN WRITTEN ON THE MAG TAPE. THE PROGRAM SHOWN BELOW CONSIST OF A VERY SIMPLE "EDITOR" PROGRAM THAT ALLOWS THE OPERATOR TO PLACE INFORMATION INTO A "BUFFER" AREA IN MEMORY. THE "BUFFER" IN THIS CASE IS LIMITED TO ONE PAGE OF MEMORY IN AN 8008 SYSTEM. WHENEVER DESIRED, THE OPERATOR CAN TRANSFER THE CONTENTS OF THE BUFFER TO THE TAPE UNIT TO CREATE A "FILE." THE PROGRAM, WHICH IS SHOWN BELOW, ASSUMES THAT THE STANDARD SCELBI TAPE READ AND WRITE PROGRAM (DESCRIBED IN THE JULY, 1975 ISSUE OF THE SCELBI DIGEST) RESIDES ON PAGE 17 IN THE SYSTEM. FURTHERMORE, IT IS ASSUMED THAN AN ASCII KEYBOARD INPUT ROUTINE AND AN OUTPUT (DISPLAY) ROUTINE IS ON PAGE 16 IN THE SYSTEM. THESE ROUTINES WOULD BE USER PROVIDED ROUTINES FOR THE USER'S PARTICULAR I/O DEVICES. NOTE THAT THE INPUT ROUTINE EXPECTS AN "ECHO" FUNCTION TO THE DISPLAY DEVICE TO OCCUR AS EACH CHARACTER IS INPUTTED SO THAT THE OPERATOR CAN VIEW DATA AS IT IS ENTERED. THE READER MAY ALSO NOTE THAT A DIFFERENT CODE WAS SUBSTITUTED FOR THE CARRIAGE RETURN AND LINE FEED FUNCTIONS. THIS WAS DONE IN THE EXAMPLE TO PROVIDE AN ILLUSTRATION OF THE TECHNIQUE BECAUSE CERTAIN TYPES OF DISPLAY DEVICES MIGHT HAVE TO PERFORM DIFFERENT FUNCTIONS IN ORDER TO EMULATE THOSE PROCESSES. FOR INSTANCE, A CRT DISPLAY MIGHT NEED TO RECEIVE SEVERAL NEW DIRECTIVES WHEN A CARRIAGE RETURN CODE WAS DETECTED IN ORDER TO POSITION THE DISPLAY TO A NEW LINE. ONE COULD THUS SUBSTITUTE AN APPROPRIATE ROUTINE WHENEVER A CARRIAGE RETURN CODE WAS DETECTED INSTEAD OF MAKING THE SIMPLE SUBSTITUTION ILLUSTRATED. OR, ONE MIGHT DESIRE TO "IGNORE" A LINE FEED, IN WHICH CASE ONE COULD MODIFY THE PROGRAM ACCORDINGLY.

THE FILE WRITE PROGRAM IS ILLUSTRATED RESIDING ON PAGE 15 WITH PAGE 14 BEING USED AS THE DATA BUFFER. OF COURSE, THE READER MIGHT DESIRE TO MODIFY THE PROGRAM TO USE A LARGER (OR SMALLER) BUFFER AREA. (THIS ARTICLE IS INTENDED TO ILLUSTRATE THE CONCEPTS INVOLVED, AND WHILE THE VERSION PRESENTED DOES OPERATE, IT IS ASSUMED THAT VARIOUS READERS WILL GO ON TO CREATE MORE SOPHISTICATED, CUSTOM TAILORED VERSIONS.)

015 000	106 156 015	START, CAL CRLF	/PROVIDE INITIAL CR&LF
015 003		/	/
015 003	106 136 015	NEWONE, CAL CLEAR	/CLEAR BUFFER AREA (000)
015 006	360	LLA	/SET REG L TO ZERO
015 007	056 014	LHI 014	/****BUFFER PAGE
015 011		/	/
015 011	106 000 016	NEXT, CAL ECHOIN	/FETCH CHAR WITH ECHO
015 014	074 215	CPI 215	/SEE IF CODE FOR CR
015 016	110 023 015	JFZ NOTCR	/SKIP NEXT IF NOT CR
015 021	006 074	LAI 074	/SUBSTITUTE FOR CR CODE
015 023		/	/
015 023	074 212	NOTCR, CPI 212	/SEE IF CODE FOR LF
015 025	110 032 015	JFZ NOTLF	/SKIP NEXT IF NOT LF
015 030	006 076	LAI 076	/SUBSTITUTE FOR LF
015 032		/	/
015 032	074 203	NOTLF, CPI 203	/SEE IF CTRL "C"
015 034	150 000 015	JTZ START	/"CLEAR" BUFFER IF CTRL "C"
015 037	074 213	CPI 213	/SEE IF CTRL "K"
015 041	150 116 015	JTZ WRITIT	/WRITE A FILE ON TAPE IF SO
015 044	074 217	CPI 217	/SEE IF CTRL "O"
015 046	110 071 015	JFZ PACK	/PUT CHAR IN BUFFER IF NOT
015 051	306	LAL	/ERASE PREVIOUS CHAR IF
015 052	240	NDA	/A CTRL "O" - BUT IGNORE THE
015 053	150 011 015	JTZ NEXT	/COMMAND IF AT LOCATION ZERO
015 056	250	XRA	/IN THE BUFFER
015 057	061	DCL	/DECREMENT POINTER TO PREV
015 060	370	LMA	/ENTRY AND CLEAR IT
015 061	006 337	LAI 337	/PRINT "-" AS ERASE
015 063	106 200 016	CAL SEND	/INDICATOR
015 066	104 011 015	JMP NEXT	/CONTINUE INPUTTING CHARS
015 071		/	/
015 071	370	PACK, LMA	/PUT CHAR IN BUFFER
015 072	240	NDA	/CLEAR CARRY BIT
015 073	306	LAL	/MOVE PNTR TO ACC
015 074	004 004	ADI 004	/SEE IF BUFFER IS ALMOST
015 076	100 112 015	JFC NEXONE	/FULL - RING BELL
015 101	106 150 015	CAL BELL	/IF SO
015 104	306	LAL	/THEN CHECK TO SEE IF
015 105	004 002	ADI 002	/REALLY FILLED - IF SO
015 107	150 116 015	JTZ WRITIT	/WRITE BUFFER TO TAPE
015 112		/	/
015 112	060	NEXONE, INL	/ELSE ADVANCE BUFFER PNTR
015 113	104 011 015	JMP NEXT	/AND GET ANOTHER CHARACTER
015 116		/	/
015 116	106 150 015	WRITIT, CAL BELL	/RING BELL AT START OF WRITE
015 121	346	LEL	/MOVE BUFFER PNTRS TO D & E
015 122	335	LDH	/TO MARK END OF FILE POINT
015 123	066 000	LLI 000	/SET POINTER TO START OF
015 125	106 147 017	CAL WRITE	/BUFFER AND WRITE TO TAPE
015 130	106 150 015	CAL BELL	/RING BELL AT FINISH OF WRITE
015 133	104 003 015	JMP NEWONE	/PREPARE BUFFER FOR NEW FILE
015 136		/	/
015 136	250	CLEAR, XRA	/CLEAR FILE BUFFER AREA
015 137	360	LLA	/BY SETTING ACC TO ZERO
015 140	056 014	LHI 014	/****AND INITIALIZE POINTER

015 142	370	NOTDON, LMA	/THEN DEPOSIT ZEROS IN BUFFER
015 143	060	INL	/MEMORY AREA UNTIL
015 144	053	RTZ	/FINISHED ENTIRE PAGE
015 145	104 142 015	JMP NOTDON	/YES - THE WHOLE PAGE!
015 150		/	
015 150	006 207	BELL, LAI 207	/SET ASCII CODE FOR BELL
015 152	106 200 016	CAL SEND	/SEND TO OUTPUT DEVICE
015 155	007	RET	
015 156		/	
015 156	006 215	CRLF, LAI 215	/PROVIDE CR & LF
015 160	106 200 016	CAL SEND	/BY FIRST SENDING CODE
015 163	006 212	LAI 212	/FOR CR AND THEN CODE
015 165	106 200 016	CAL SEND	/FOR LF
015 170	007	RET	
		/	

TO CREATE FILE(S), THE PROGRAM IS STARTED (PAGE 015 LOCATION 000). THE AUDIO TAPE RECORDER SHOULD BE CONNECTED TO THE TAPE INTERFACE WITH THE MOTOR CONTROL OPTION BEING USED. THE SIMPLE "EDITOR" PORTION OF THE PROGRAM USES THE FOLLOWING SPECIAL "CONTROL FUNCTIONS" TO DIRECT OPERATION OF THE PROGRAM FROM THE USER'S INPUT DEVICE (SUCH AS A KEYBOARD.)

"CONTROL/C" ("CONTROL" AND LETTER "C" DEPRESSED SIMULTANEOUSLY) RESULTS IN THE INPUT BUFFER BEING CLEARED TO THE ALL ZERO CONDITION. IT SERVES AS AN EASY WAY TO ERASE THE BUFFER SHOULD THE OPERATOR DISCOVER AN ERROR WHILE ENTERING DATA.

"CONTROL/O" SERVES TO DELETE THE PREVIOUS CHARACTER ENTERED BY THE OPERATOR FROM THE BUFFER. IT MAY BE USED MORE THAN ONCE TO DELETE SEVERAL INCORRECT CHARACTERS. A BACK ARROW IS DISPLAYED EACH TIME THIS FUNCTION IS USED. THE FUNCTION IS INTENDED AS A SIMPLE "EDITING" CAPABILITY FOR CORRECTING MINOR "TYPO" ERRORS.

"CONTROL/K" CAUSES THE CURRENT CONTENTS OF THE BUFFER TO BE WRITTEN ONTO THE TAPE UNIT TO CREATE A BLOCK OR "FILE." THE BUFFER IS THEN AUTOMATICALLY "CLEARED" TO PREPARE FOR A NEW ENTRY. AT THE START AND AT THE END OF THE ACTUAL FILE WRITING PROCESS, A "BELL" IS RUNG (IF A TTY UNIT IS IN USE) TO INDICATE TO THE OPERATOR THE START AND END OF THE ACTUAL TAPE WRITE PROCESS.

THE OPERATOR DOES NOT HAVE TO USE THE "CONTROL/K" COMMAND TO SEND A FULL BLOCK OF DATA TO THE TAPE UNIT. THE PROGRAM ILLUSTRATED WILL AUTOMATICALLY TRANSFER DATA TO THE TAPE UNIT WHEN THE BUFFER IS FILLED WITH 256 (DECIMAL) CHARACTERS. FURTHERMORE, AS THE BUFFER APPROACHES IT'S CAPACITY, THE "BELL" (ON A TTY) IS RUNG TO WARN THE OPERATOR TO "SLOW DOWN" THE INPUT PROCESS. (A GOOD TYPIST COULD TYPE THREE OR SO CHARACTERS AFTER THE TAPE UNIT STARTED BUT BEFORE REFLEXES RESPONDED TO THE "BELL" AT THE START OF THE WRITE CYCLE IF NO WARNING WAS GIVEN!)

A SIMPLE FILE READ PROGRAM IS ILLUSTRATED AT THE TOP OF THE NEXT PAGE. THE PROGRAM SHOWN SIMPLY READS IN EACH FILE FROM THE TAPE UNIT INTO THE BUFFER AREA AND THEN DISPLAYS THE CONTENTS OF THE BUFFER. FOR THE VERSION SHOWN IT IS ASSUMED THAT THE DISPLAY DEVICE IS A TTY. AS SOON AS THE DATA HAS BEEN PRINTED, THE PROGRAM GOES ON TO READ IN ANOTHER FILE. THIS PROGRAM IS ONLY INTENDED AS A FRAMEWORK FROM WHICH THE READER MAY PROCEED TO BUILD UP A MORE SOPHISTICATED SYSTEM. A FEW COMMENTS ON EXPANDING THE PROGRAM'S CAPABILITY TO IMPLEMENT A "CHECK AND SKIP" FILE SYSTEM WILL BE PRESENTED NEXT.



```

/
015 200 106 210 017 FREAD, CAL READ /READ A FILE FROM TAPE
015 203 250 XRA /CLEAR ACCUMULATOR
015 204 360 LLA /SET PNTR BACK TO START
015 205 056 014 LHI 014 /****BUFFER PAGE
015 207 /
015 207 307 CHRFBT, LAM /OF FILE & FETCH A CHAR
015 210 240 NDA /SET FLAGS AFTER LOAD
015 211 150 200 015 JTZ FREAD /IF "000" GET NEXT FILE
015 214 074 074 CPI 074 /SEE IF CODE "CR"
015 216 110 226 015 JFZ NOCR /SKIP NEXT IF NOT
015 221 006 215 LAI 215 /IF SO, SUBSTITUTE CR
015 223 104 235 015 JMP PRINT /AND DISPLAY
015 226 /
015 226 074 076 NOCR, CPI 076 /SEE IF CODED "LF"
015 230 110 235 015 JFZ PRINT /SKIP NEXT IF NOT
015 233 006 212 LAI 212 /IF SO, SUBSTITUTE LF
015 235 /
015 235 106 200 016 PRINT, CAL SEND /DISPLAY CHARACTER
015 240 /
015 240 060 AHEAD, INL /ADVANCE BUFFER PNTR
015 241 104 207 015 JMP CHRFBT /AND CONTINUE PROCESS
/

```

TO IMPLEMENT A "CHECK AND SKIP" CAPABILITY ONE WOULD SIMPLY PROCEED TO ESTABLISH A CODING CONVENTION WHEN FILES WERE WRITTEN AND THEN ADD A SUBROUTINE TO THE FILE READ PROGRAM TO TEST FOR A DESIRED CONDITION. SUPPOSE, FOR INSTANCE, ONE HAD A CLUB MAILING LIST WHERE MEMBERS COULD BELONG TO ANY ONE (OR MORE) SPECIAL INTEREST GROUPS. ONE COULD USE THE COMPUTER TO SELECT INDIVIDUALS WHO WERE TO RECEIVE SPECIAL INTEREST NEWS BY USING THE FOLLOWING TECHNIQUE.

ON THE FIRST LINE OF THE DATA BLOCK CONTAINING THE MEMBERS NAME AND ADDRESS, ASSIGN A LETTER OR NUMBER CODE TO REPRESENT EACH SPECIAL INTEREST GROUP THAT THE MEMBER WAS ACTIVE IN. THUS, AN ENTRY MIGHT APPEAR AS:

```

AEGH
JOHN DOE
123 MAIN ST.
ANYTOWN, US 12345

```

WHERE THE LETTERS A, E, G AND H ON THE FIRST LINE REPRESENTED THE CODES FOR VARIOUS SPECIAL INTEREST GROUPS THAT THE MEMBER PARTICIPATED IN.

TO PROCESS SUCH A SYSTEM, ONE WOULD SIMPLY NEED TO MODIFY THE READ PROGRAM ABOVE (SAY, BY CALLING A SUBROUTINE JUST BEFORE "CHRFBT") SO THE FIRST LINE OF AN ENTRY WAS SCANNED FOR A PARTICULAR CODE REPRESENTING A GROUP THAT WAS TO BE INCLUDED IN THE CURRENT MAILING. IF THE DESIRED CHARACTER WAS FOUND, THEN THE PROGRAM COULD PROCEED TO PRINT THE REST OF THE FILE (STARTING WITH THE NEXT LINE!) AS THE NAME AND ADDRESS. OTHERWISE, NO PRINT OUT WOULD BE REQUIRED, AND THE PROGRAM WOULD CONTINUE BE IMMEDIATELY PROCEEDING TO READ IN ANOTHER FILE FROM THE TAPE UNIT.

ONE MIGHT NOW BE ABLE TO SEE THAT THE CONCEPT CAN THEN BE EXPANDED TO ALLOW, SAY, MULTIPLE INTEREST GROUPS TO BE SELECTED (BY PERFORMING A "LOGICAL AND" TEST) OR COMBINATIONS OF GROUPS. ONE COULD, IN FACT, EXPAND THE READ PROGRAM INTO A FULL BLOWN PROGRAM TO ENABLE AN UNSKILLED OPERATOR TO DEFINE THE SELECTION CRITERIA! GOT SOME IDEAS NOW?

MR. WILLARD I. NICO, OF DELTA T, 11020 OLD KATY ROAD, SUIT 204, HOUSTON, TX. 77043, SENT IN TWO CONTRIBUTIONS. THE FIRST IS A MODIFICATION TO THE SCELBI-8H THAT ALLOWS THE PROCESSOR TO WAIT DURING I/O CYCLES FOR A PERIPHERAL DEVICE TO INDICATE THAT IT IS "READY." THE SECOND CONTRIBUTION IS A ROUTINE THAT CONVERTS BINARY NUMBERS STORED IN A SINGLE REGISTER TO IT'S DECIMAL EQUIVALENT. THANKS FOR TAKING THE TIME TO SHARE YOUR CREATIONS WITH OTHERS, MR. NICO.

MODIFICATIONS TO SCELBI CPU CARD TO ALLOW PROCESSOR TO "WAIT" DURING INPUT AND OUTPUT CYCLES FOR A PERIPHERAL THAT IS NOT READY.

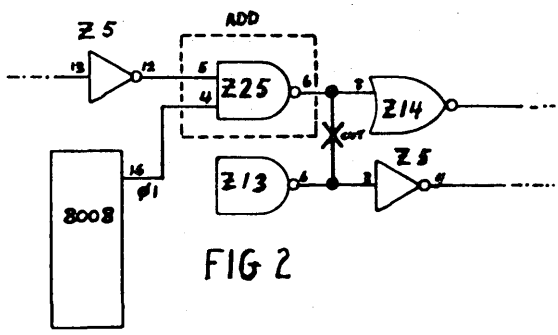
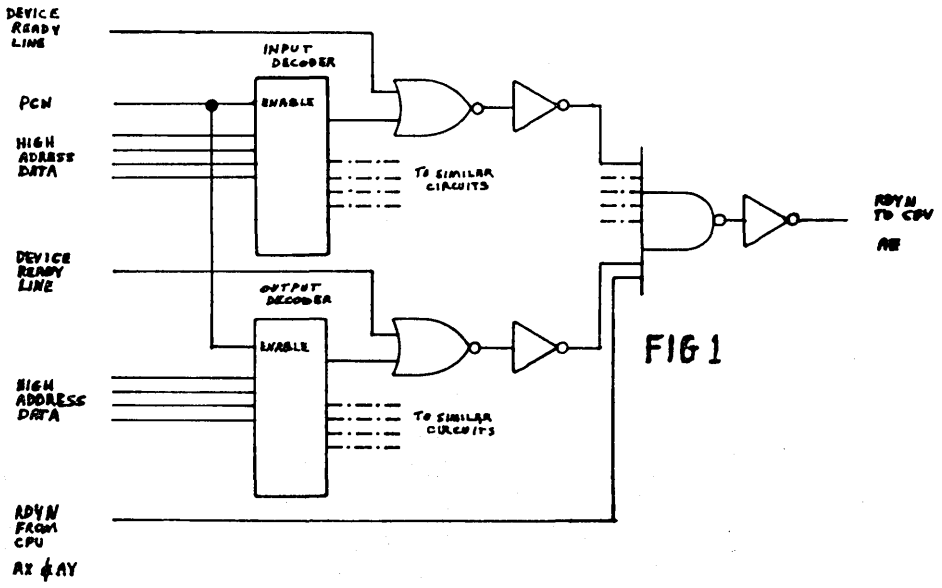
#### THEORY

The "Interrupt" provisions of the 8008 CPU are useful in many circumstances, but not so useful when a dedicated program is being run with asynchronous input and/or output requirements. For example, a routine to simply copy a paper tape must wait until the reader has finished cycling from the last input strobe before it can fetch the new byte. Similarly, the routine must wait for the punch to finish cycling from the last output before a new punch command can be issued. While this waiting is going on, there is nothing the computer can "be off somewhere doing" while waiting for an interrupt.

Certain timing provisions of the Scelbi 8H CPU card do not allow for the CPU to wait in this manner, but they can be easily modified, and the extra gates required for the modifications are "extras" that remain unused on the standard CPU card.

#### INPUT AND OUTPUT "WAIT" CIRCUIT

There are many ways to configure the peripheral control interface circuits. The circuit shown in Figure 1 monitors data from the high address latches and drives a select line "low" when an input or output command is decoded. The select line is "NOR'd" with the READY line from the selected peripheral and after inversion, combining with other similar circuits and the RDYN line from the CPU card, is returned as the new RDYN output.



## THE PROBLEM

While Figure 1 looks good on paper and should work, it didn't. The device identification is strobed into the high address latches at T2 time and may be extracted by enabling the decoders with the PCN signal from the CPU card (pin B-12).

The problem is that the High Address Strobe (HAS on pin B-19 of CPU card) occurs at clock  $\phi_{22}$  and the 8008 must have the READY line at logic "0" prior to  $\phi_{22}$  of T2 to guarantee entry into the WAIT state. (See note 1 on page 23 of INTEL 8008 Users Manual, November 1973, Revision 4).

An investigation of the timing chart (above reference) shows that the data for the High Address latches is valid one clock pulse earlier than  $\phi_{22}$ , which is  $\phi_{12}$ . By making the modification shown in Figure 2, the device identification will be strobed into the High Address latches earlier so that it can be decoded and the READY line brought to logic "0" prior to  $\phi_{22}$  if the device is not ready.

## A SECOND PROBLEM

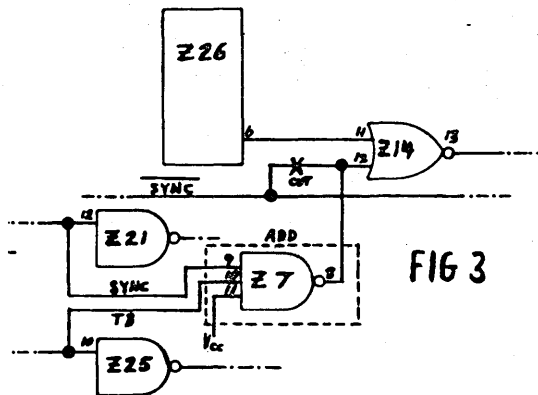
After making the above modification (it's easy), you will find that the circuit still doesn't work! It won't wait for a slow peripheral the first time you address it, but does seem to wait the second time. This can be fixed just as easily.

This problem is caused by the Z26 "anticipation" circuit. It's needed so that everything is ready to go at the very beginning of T3 time instead of having to wait for the first available clock pulse, which is  $\phi_{21}$ . But the trouble is, all conditions are "GO" at the last gasp of T2 time and the Input or Output strobe gets generated just as T2 waves goodbye.

Obviously, it doesn't do any good to enter a wait state between T2 and T3 if the deed has already been done. So the strobes get generated and the computer waits after a strobe which went out while the device was still busy with the one before.

The fix is to hold off on the INP and OUT strobes until the CPU gets to T3 time and after it has done any necessary waiting.

The circuit of Figure 3 uses another spare gate to add T3 time information to the strobe generating circuits.



ROUTINE FOR CONVERTING BINARY CONTENTS  
OF "E" REGISTER TO THREE DECIMAL DIGITS  
(WITH LEADING ZERO SUPPRESSION) AND OUTPUTTING.

Note: Addresses follow "Monitor 8" software convention of six digit group with page number first.

Note: Restart 2 (RST020) is User's output routine.

001000/ 036 LDI 060	Load ASCII number code for zero in "D" register
001002/ 323 LCD	And Register "C"
001003/ 313 LBD	And Register "B"
001004/ 304 LAE	Get number to be converted
001005/ 074 CPI 000	Is it zero?
001007/ 150 JTZ 001061	If so, go print a single zero
001012/ 006 LAI 072	Set up A with ASCII zero plus ten
001014/ 030 IND	Tally one in "D" Register (Least significant digit)
001015/ 273 CPD	Did that get D to "ten" decimal?
001016/ 110 JFZ 001033	If not, go keep score in "E" Register
001021/ 036 LDI 060	If so, reset "D" to ASCII zero
001023/ 020 INC	And add one (carry) to "C"
001024/ 272 CFC	Did that get "C" to "ten" decimal?
001025/ 110 JFZ 001033	If not, keep score
001030/ 026 LCI 060	If so, reset "C" to ASCII zero
001032/ 010 INB	Carry to "B"
001033/ 041 DCE	Decrement "E"
001034/ 110 JFZ 001014	Not done yet; loop back
001037/ 301 LAB	All done. Get most significant digit

001040/ 074 CPI 060	Is it zero (ASCII)?
001042/ 110 JFZ 001056	No. Go print all three digits
001045/ 302 LAC	Yes. How about middle digit?
001046/ 074 CPI 060	Is it at zero (ASCII)?
001050/ 110 JFZ 001060	No. Go print last two digits
001053/ 104 JMP 001061	Yes it is. Print least significant digit only.
001056/ 025 RST020	Come here to print most significant digit
001057/ 302 LAC	Get middle digit
001060/ 025 RST020	And print it
001061/ 303 LAD	Get least significant digit
001062/ 025 RST020	And print it
001063/ 007 RET	Go home

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THE NAVAL ADMIRAL HAD JUST PURCHASED A MINICOMPUTER TO HELP HIM RUN HIS MIGHTY FLEET. HE QUICKLY UNPACKED HIS UNIT, SET IT UP IN HIS STATE ROOM, PLUGGED IT IN, AND WITHOUT WASTING ANY TIME, PROCEEDED TO ASK HIS NEW COMPUTER AN IMPORTANT QUESTION.

"WILL THE WEATHER BE SUITABLE FOR LAUNCHING PLANES FROM MY AIRCRAFT CARRIER TOMORROW - OR WILL IT RAIN?"

"YES.." ANSWERED HIS NEW LITTLE BRAIN..

"YES WHAT?" SHOUTED THE EXASPERATED ADMIRAL..

"YES SIR!!" PIPED UP HIS LITTLE MINI..

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